

Abstract

Capacitor structures for use in integrated circuits and methods of their manufacture. The capacitor structures include a bottom electrode, a top electrode and a dielectric layer interposed between the bottom electrode and the top electrode. The capacitor structures further include a metal oxide buffer layer interposed between the dielectric layer and at least one of the bottom and top electrodes. Each metal oxide buffer layer acts to improve capacitance and reduce capacitor leakage. The capacitors are suited for use as memory cells and apparatus incorporating such memory cells, as well as other integrated circuits.

"Express Mail" mailing label number: EL61847772US
Date of Deposit: December 20, 2000

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.